WHAT IS CLAIMED IS:

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1. A processor comprising:

means for executing an instruction of an application of a first bit size ported to a second bit size environment, the second bit size being greater than the first bit size; and

means for confining the application to a first bit size address space subset.

2. The processor of claim 1, wherein the first bit size is 32-bit and the second bit size is 64-bit.

3. The processor of claim 1, wherein the means for confining includes:

means for truncating generated address references of the second bit size to the first bit size; and

means for extending to the second bit size the truncated generated address references.

4. The processor of claim 3, wherein the means for confining includes means for generating an address fault.

5. The processor of claim 1,wherein the means for extending includes means for determining that the first bit size address space subset is signed address space.

6. The processor of claim 1,wherein the means for extending includes means for determining that the first bit size address space subset is unsigned address space.

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7. A processor comprising:

a memory to store an instruction of an application ported from a first bit size environment to a second bit size environment, the second bit size being greater than the first bit size; and

an instruction execution core coupled to said memory, said instruction execution core to execute the instruction of the application, said instruction execution core to

determine that the application is confined a first bit size address subset;

generate an address reference of the second bit size as part of execution of the instruction;

truncate the generated address reference from the second bit size to the first bit size; and

extend the truncated, generated address reference from the first bit size to the second bit size.

8. The processor of claim 7, wherein the application ported from a first bit size environment to a second bit size environment is an application ported from a 32-bit environment to a 64-bit environment.

9. The processor of claim 7, wherein the instruction execution core is to determine that the application is confined to a first bit size address subset based at least in part on an address space control flag.

10. The processor of claim 7, wherein the instruction execution core is to extend the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag.

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11. The processor of claim 7, wherein the instruction execution core is to generate an address fault flag based least in part on a comparison of the generated address reference and the extended, truncated, generated address reference.

12. The processor of claim 11, wherein the instruction execution core is to generate an address fault flag based least in part on an address fault control flag.

13. The processor of claim 7, wherein said memory is a cache memory.

14. The processor of claim 7, wherein the processor is a 64-bit processor.

15. A method to confine an application to an address space subset, the method comprising:

determining that an application is confined a first bit size address subset, the application including an instruction;

generating an address reference of the second bit size as part of execution of the instruction;

truncating the generated address reference from the second bit size to the first bit size; and

extending the truncated, generated address reference from the first bit size to the second bit size.

16. The method of claim 15, wherein the application is ported from a first bit size environment to a second bit size environment.

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17. The method of claim 16, wherein the application ported from a first bit size environment to a second bit size environment is an application ported from a 32-bit environment to a 64-bit environment.

18. The method of claim 15, wherein determining that an application is confined a first bit size address subset, the application including an instruction is based at least in part on a address space control flag.

19. The method of claim 15, wherein extending the truncated, generated address reference from the first bit size to the second bit size is based at least in part on an address format control flag.

20. The method of claim 15, wherein extending the truncated, generated address reference from the first bit size to the second bit size includes sign-extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag.

21. The method of claim 15, wherein extending the truncated, generated address reference from the first bit size to the second bit size includes zero-extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag.

22. The method of claim 15, wherein extending the truncated, generated address reference from the first bit size to the second bit size includes generating an address fault flag based least in part on a comparison of the generated address reference and the extended, truncated, generated address reference.

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23. The method of claim 22, wherein generating an address fault flag is based least in part on an address fault control flag.